

REMARKS

Claims 1-11 remain pending. Claims 5, 7, 9, and 11 are currently amended for clarification. No claims are canceled or added.

Claim 11 stands objected to as having an unclear final paragraph. As shown above, applicant amends the text of that paragraph thereby causing it to become clear. Accordingly, withdrawal of the objection is now requested.

Although not specifically stated, it is implied in the Office Action that claim 11 is rejected under 35 U.S.C. § 112, second paragraph, as indefinite for reciting “the reference frequency divided signal” without antecedent basis.

Regretfully, applicant unintentionally neglected to file in the original version of the claim the antecedent basis for “the reference frequency divided signal.” As shown above, claim 11 is amended to include the omitted text, including the antecedent basis of “the reference frequency divided signal.” Accordingly, withdrawal of the indefiniteness rejection is now requested.

Claims 1-11 stand rejected under 35 U.S.C. § 102(e) as anticipated by *Jokura* (U.S. Patent No. 6,173,025). Applicant respectfully traverses this rejection. *Jokura* does not teach all the subject matter recited in the claims, as explained in the following:

Claim 1 describes a method that includes the step of generating a power saving state canceling signal “in accordance with the reference frequency divided signal and the comparison frequency divided signal.” Claim 2 depends from claim 1, so it also describes this subject matter.

Claims 3, 5, 7, and 9 describes apparatuses that include a canceling signal generator, which generates a power saving state canceling signal “in accordance with the reference frequency divided signal and the comparison frequency divided signal.” Claims 4, 6, 8, and 10 depend from claims 3, 5, 7, and 9, respectively, so they also describe this subject matter.

The rejection relies on divide-by-N frequency divider 9 to teach a “reference signal frequency dividing unit” and on divide-by-M frequency divider 3 to teach a “comparison signal dividing unit.” Applicant acknowledges the *Jokura* disclosure in column 1, lines 18-24, that power saving is sometimes an important feature of a phase-locked loop.

However, to anticipate the claims, *Jokura* would need to disclose not only entering a power saving state but also leaving the power saving state. Additionally, *Jokura* would need to disclose that the signal canceling the power saving state is generated “in accordance with the reference frequency divided signal and the comparison frequency divided signal.” Applicant finds no teaching in *Jokura* of resuming the power to frequency dividers 3 and 9 based their output signals. The Office Action only provides a citation of switch 5 and control circuit 10 as supposedly teaching this claim feature. However, although these elements might be used for resuming the power to frequency dividers 3 and 9, the Office Action does not explain how a decision to resume the power is based the output signals of frequency dividers 3 and 9. Therefore, the rejection of claims 1-10 has not been justified.

Regarding claim 11, this claim describes a method that includes the following two steps:

generating a power saving state canceling signal with the reference frequency divided signal so as to output a comparison result; and

generating an initializing signal for initializing the dividing of the frequency of the reference signal or the frequency of the input signal in accordance with the power saving state canceling signal.

To justify the rejection of claim 11, the Office Action only references control circuit 10 of *Jokura* as the explanation that the first of the above-quoted steps are anticipated. Regarding the second step, the Office Action only cites gate circuits 2 and 8.

In the *Jokura* circuit, a power saving pulse is supplied to control circuit 10 and two signals are supplied from the control circuit to gates circuits 2 and 8 provided immediately

before frequency dividers 3 and 9, respectively, to stop them from operating. That is, the *Jokura* circuit merely stops the supply of input signals to the frequency dividers. This is not a teaching of generating an initializing signal in the manner recited in claim 11, and thus the rejection should be withdrawn.

In accordance with the present invention, when under the power-saving operation control of a PLL circuit, after confirmation of changes in the outputs of a reference signal frequency dividing circuit and a comparison signal dividing circuit, the power saving state can be canceled positively and stably by setting the phase difference of the two input signals to the phase comparator to be less than a predetermined value by using two initializing signals.

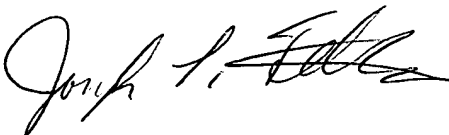
In view of the remarks above, applicant now requests the withdrawal of the anticipation rejection of claims 1-11.

In a separate matter, applicant notes that the Office Action does not indicate review of the Information Disclosure Statement (IDS) filed September 2, 2003. Applicant requests that the next communication from the PTO indicate such review.

In view of the remarks above, applicant now submits that the application is in condition for allowance. Accordingly, a Notice of Allowability is hereby requested. If for any reason it is believed that this application is not now in condition for allowance, the Examiner is welcome to contact applicant's undersigned attorney at the telephone number indicated below to discuss resolution of the remaining issues.

If this paper is not timely filed, applicant petitions for an extension of time. The fee for the extension, and any other fees that may be due, may be debited from Deposit Account No. 50-2866.

Respectfully submitted,
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Enclosure: Petition for extension of time

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